

3D Network Structures using Circuit Switches and Packet Switches for on-chip Data Centers

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Abstract—The energy consumption of the data center becomes a great problem. One approach to reducing the energy consumption of the data center is to use *on-chip data centers*, which are integrated circuit chips that perform the tasks in a data center. On-chip data centers are constructed of cores and the network between cores. Because the tasks are performed by the cooperation between cores in the on-chip data center, the network between cores in the on-chip data center may have a large impact on the performance and the energy consumption of the chip. In this paper, we investigate the network structures for the on-chip data centers. We focus on the 3D network structure using both circuit and packet switches, and compare the energy consumption of the candidate network structures. The results show that (1) the packet switches connected to cores should be placed in the same layer, (2) the packet switches should connect to the circuit switches in all layers, and (3) each layer should include only the minimum number of switches regardless of the traffic pattern, the size of the chip, and the ratio of the energy consumption of the packet and circuit switches.

Keywords—*network on-chip; data center; energy consumption; topology; 3D on-chip network*

I. INTRODUCTION

One approach to reducing the energy consumption is to use the *on-chip data centers*, which are integrated circuit chips that perform the tasks in a data center. Because the network between cores in the on-chip data center may have a large impact on the performance and the energy consumption of the chip, we investigated the network structures suitable for the on-chip data center [1]. In this paper, in addition to the above results discussed on the previous version of this paper [1], we also investigate the impact of the traffic pattern, the size of the chip, and the ratio of the energy consumption of the packet and circuit switches on the suitable network structure.

In recent years, online services such as cloud computing have become popular, and the amount of data, required to be processed by such online services, is increasing. Such a large amount of data is handed by data centers, and many data centers have been built [2],[3]. As the services provided by data centers become popular, the energy consumption of the data centers becomes an important problem; the energy consumed by data centers occupies 1.5 % of the total energy consumption consumed in the world [3].

One approach to reduction of the energy consumption caused by the data centers is an integrated circuit chip that can perform the tasks in a data center. This kind of chip is called an *on-chip data center* [4],[5]. An on-chip data center is made of a large number of CPU cores and the network between the cores on a single chip. An on-chip data center works with a significantly small energy because of its small wiring length of the network within a chip [4].

Most of existing work on on-chip data centers focus on the usage of many cores on the chip. However, because tasks in a data center require communication between servers, the network structures between cores may have a large impact on the performance and/or the energy consumption of the on-chip data center.

The network within a chip is often called a *Network on-chip (NoC)*, and constructed of switches [6],[7]. Two types of switches are used in a NoC, packet switches and circuit switches.

A packet switch relays packets, based on their destination addresses. On the other hand, a circuit switch connects its input port with one of its output ports based on the configuration. A circuit switch consumes a small energy compared with a packet switch because it does not require any processing to relay traffic, though multiple flows from different input ports cannot share the same output port.

Several NoC architectures that use both packet and circuit switches have been proposed [6],[8],[9]. In these architectures, the circuit path between packet switches is established by configuring the circuit switches along the route of the circuit path. The set of the packet switches and the established circuit paths constructs the logical network topology. In these architectures, the logical network topology can be changed by the configuration of the circuit switches. Stensgaard et al. [9] proposed a method to configure the circuit switches suitable to the application before starting the application.

The network architectures using both of packet and circuit switches are also effective in an on-chip data center. In a data center, though the traffic pattern changes significantly and frequently, each server communicate with only a small number of servers at once [10]. Considering such traffic, the logical topology where the communicating server pairs are connected closely is preferable. This network topology can be set by setting the circuit switches in the network using both of the packet and circuit switches. Even if the traffic pattern changes, we change the network topology so as to suit the current traffic pattern by reconfiguring the circuit switches.

In recent years, another new NoC architecture called *3D NoC* has been proposed [s7,ron2,ron3,ron4]. The 3D NoC is constructed by stacking multiple 2D chip layers vertically. The vertically stacked layers decrease the number of hops between switches. Moreover, the vertical links of the 3D NoC are significantly shorter than the horizontal links. As a result, the 3D NoC reduces both of the energy consumption and latency.

In addition, the 3D NoC improves the effectiveness of using packet and circuit switches. Because the 3D NoC increases the number of candidate routes of the circuit paths, more circuit paths are established, which reduce the energy consumption.

However, the 3D NoC using both packet and circuit switches has not been discussed sufficiently.

We investigated the network structures suitable for the on-chip data center [1]. In this investigation, a server in an on-chip data center is constructed by multiple directly connected cores. Then, the network connects the servers.

We focused on the network constructed as a 3D network using circuit and packet switches. We investigated the network structures, focusing on the following three points; (1) connection between layers in the 3D network, (2) connection between servers and switches, and (3) placement of switches within each layer. The results show that (1) all servers should be connected to the packet switches in the same layer, (2) all packet switches should be connected to all layers, and (3) each layer should include minimum number of switches.

In addition to the above results discussed on the previous version of this paper [1], the network structures are compared, changing the traffic pattern, the size of the chip, and the ratio of the energy consumption of the packet and circuit switches. Through this evaluation, we show that our discussion on the suitable network structure is applicable regardless of the traffic pattern, the size of the chip, and the ratio of the energy consumption of the packet and circuit switches.

The rest of this paper is organized as follows. Section II explains the overview of the on-chip data center used in this paper. In Section III, we investigate the network structures suitable to the on-chip data center. Section IV presents the conclusion.

II. ON-CHIP DATA CENTER NETWORK

A. The Outline Of On-Chip Data Center

The on-chip data center is a chip that plays the roles of the servers and network between servers in a data center. The on-chip data center is constructed of cores and the network between cores. Similar to the traditional data center, where a task handling a large amount of data is performed by the cooperation of the servers [11],[12], the tasks in an on-chip data center are performed by cores cooperating with each other; each task is split into subtasks, and the subtasks are assigned to the cores. Each core performs the assigned subtask, and it obtains the data or the results of the other subtasks from the other cores via the network, if the data or the results are required.

The network between cores is important in the on-chip data center, because the cores cooperate with each other via the network to complete the task. The network should provide the bandwidth between communicating cores with small energy consumption. The network within the on-chip data center consumes less energy than the traditional data center network, because of its small wiring length of the network within a chip [4]. However, the energy consumption of the on-chip network depends on the network structures. Therefore, we investigate the network structures for the on-chip data center.

B. Components of On-Chip Data Center

The on-chip data center is constructed of multiple cores and a network between cores. The details of the components in the on-chip data center are described below.

1) *Core*: In the on-chip data center, there are two kinds of the cores. One is the computing core that performs the process of the assigned task. The other is the memory core that stores the data.

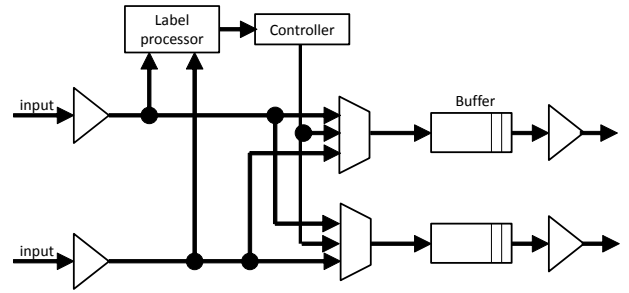


Figure. 1. Packet switch

In an on-chip data center, each task is split into multiple subtasks, and the subtasks are assigned to the computing cores. The computing core performs the assigned subtask, cooperating with multiple memory cores; the computing core reads the required data from the memory cores, and writes the results of the process to the memory cores.

As described above, the cores cooperating with each other; the results of the other computing cores may be required to complete the assigned subtask. In this case, the core obtains the required data generated by the other cores via the network between cores.

2) *Network*: The network within an on-chip data center is constructed of two kinds of switches described below.

a) *Packet Switch*: A packet switch is a switch that relays the packet based on the destination written in the header of the packet. An example of the architecture of the packet switch is shown in Figure 1. When a packet arrives, the destination written in the header of the packet are processed by the label processor. Based on the destination, the output port, to which the packet is relayed, is determined. Then, the controller configure the switch to relay the packet to the buffer deployed at the output port. Finally, the packet is sent to the next switch or core from the buffer.

The energy consumption of the packet switch increases as the number of arriving packets increases, because the processes of the label processors and the controller are performed each time a packet arrives. Moreover, writing a packet to a buffer or reading a packet from a buffer also consumes energy. Therefore, the number of packet passing the packet switches should be reduced to save the energy consumption.

b) *Circuit Switch*: A circuit switch is a switch that connects its input and output ports based on the configuration. After the configuration of the ports, all packets arriving the input port is relayed to the output port connected to the input port. An example of the architecture of the circuit switch is shown in Figure 2.

The circuit switch consumes less energy than the packet switch, because the circuit switch does not require complicated processing such as label processing and decision of the output ports. However, the circuit switch cannot relay flows from different input ports to the same output port, because each output port can be connected at most one input port in the circuit switch.

C. The Architecture of On-Chip Data Center Used in This Paper

Figure 3 shows the on-chip data center used in this paper.

In this architecture, one computing core and multiple memory cores are vertically stacked and directly connected.

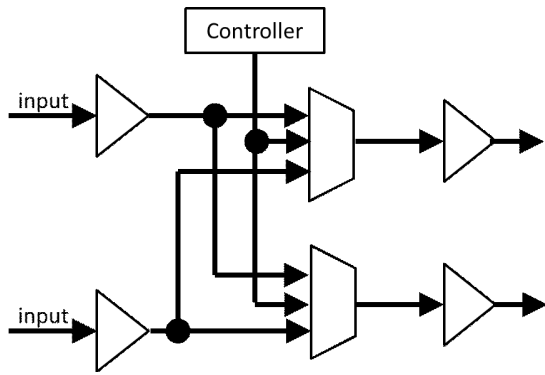


Figure 2. Circuit switch

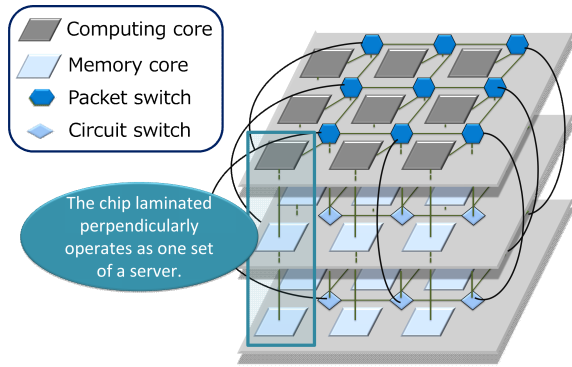


Figure 3. On-chip data center used in this paper

The connected cores act as a single server in a data center. Hereafter, the connected cores are simply called *server*.

In this architecture, the servers are placed in a lattice, and the network between servers is constructed of switches placed in a 3D lattice, because the lattice network can be easily constructed on a chip.

In this architecture, both kinds of switches, packet switches and circuit switches are used. The packet switches are deployed where there is a link from/to a server, so that each server communicates with multiple servers at once. In this paper, the same number of packet switches as the servers are deployed, and each server is connected to the network by connecting one of its cores to one of the packet switches.

Though we do not allow each packet switch to be connected to multiple servers in this paper, the discussion of the suitable network structure is applicable to the case that each packet switch can be connected to multiple servers, because connection to multiple servers has no impact except for the increase of the candidates of the first packet switch and the last packet switch on the route between the servers. The switches not connected to servers are circuit switches because the circuit switches consumes less energy.

In this network, the traffic is sent after constructing the logical network topology by setting the circuit paths between packet switches. The circuit paths are established by configuring the circuit switches along the paths. Then, the traffic is sent over the logical network topology of the packet switches constructed by the circuit paths.

This network structure has the following parameters; (1)

the connection between layers, (2) the layers where switches connected to servers are deployed, and (3) the types of switches deployed in each layer, which are discussed in Section III.

III. COMPARISON OF NETWORK STRUCTURES FOR ON-CHIP DATA CENTERS

A. Compared Network Structures

In this section, we investigate the network structures suitable to on-chip data centers by comparing the network structures constructed with various parameters. In our comparison, all network structures are constructed of packet switches with 9 ports and circuit switches with 10 ports. The number of vertical layers are set to 5.

The rest of this subsection describes how to set the parameters of the network structures in this comparison.

1) *Inter-Layer Connection*: The first parameter is the inter-layer connection. There are two types of the inter-layer connection. The first one is shown in Figure 4(a) In this type of the connection, switches in all layers are connected to the same packet switch. We call this type of connection the *packet switch centric connection (PCC)*.

The other type is shown in Figure 4(b) In this types of connection, all vertical links are constructed only between nearest layers. For example, a switch placed at the i th layer is connected only with the switches placed at the $i - 1$ th layer and the $i + 1$ th layer. This type is called of connection the *nearest layer connection (NLC)*. In the NLC, we construct the close connection between the nearest layers. All vertical links from the switches are connected to the switches at the nearest layer.

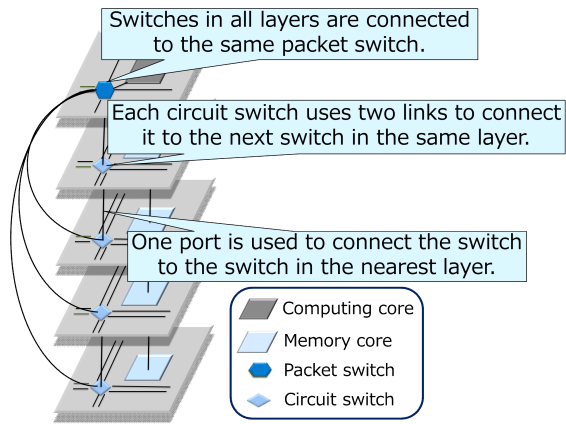
In our comparison, the PCC and the NLC use 1 of 9 port of a packet switch to connect to the server, 4 of 9 ports of each packet switch to connect the switches within the same layer, and the other ports to connect the switches at the different layers.

2) *Connection between Servers and Switches*: In the on-chip data center investigated in this paper, each server is connected to one of the packet switches nearest to the server. As shown in Figure 5, there are two types of connections between servers and switches. In the first type of the connection, all servers are connected to the switches in the same layer. We call this type of connection the *same layer connection (SLC)*. In the other type of connection, the servers neighboring with each other are connected to the switches in the different layers. We call this type of connection the *different layer connection (DLC)*.

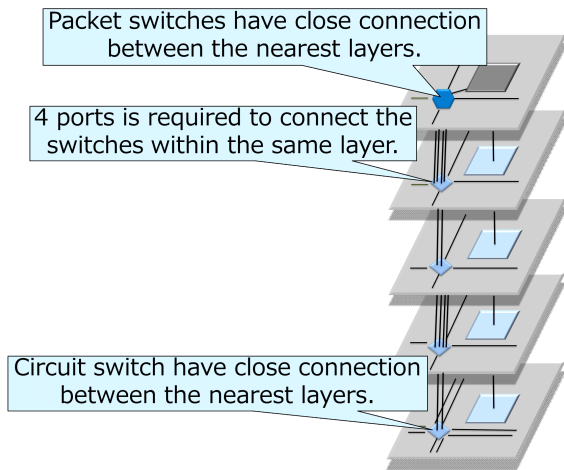
In the SLC, the number of hops between servers is small because all servers are connected in the same layer. However, the connections of packet switches at the first layer are static. On the other hand, the connections between packet switches can be changed in any layers in the DLC.

3) *Placement of Switches within a Layer*: There are two kinds of placement of the switches in the same layer. The first one is shown in Figure 6(a). In this type of the placement, we deploy the same number of switches as the number of servers in each layer. We call this type of placement *minimum placement (MP)*. In the other type of placement, we add the circuit switches around the packet switches. We call this type of placement the *additional circuit switch placement (ACP)*.

The ACP has more candidates of routes of circuit paths between the packet switches than the MP. Thus, the energy efficient routes may be found, even when the number of circuit



(a) Packet switch centric connection



(b) Nearest layer connection

Figure 4. Inter layer connection

path to be established is large. However, the number of circuit switches passed by each circuit path in the ACP is larger than that in the MP.

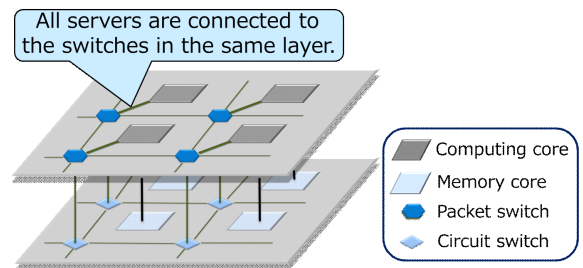
B. Models Used in Our Comparison

1) *Energy consumption model*: The energy consumed by the network on-chip depends on (1) network structure, (2) the traffic amount on the network, and (3) the bit flips of the traffic.

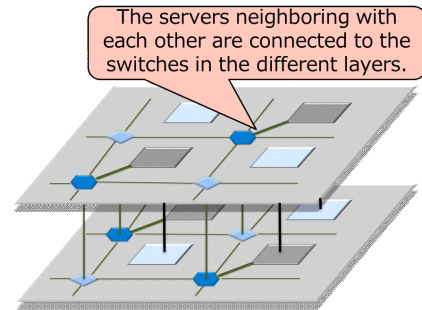
Wolkotte et al. [13] model the energy consumed by a circuit switch, a packet switch and a link in the NoC. In this model, the circuit switch consumes $E^{\text{packet}} \mu\text{W}$, the packet switch consumes $E^{\text{circuit}} \mu\text{W}$, and the link consumes $(E^{\text{stlink}} + E^{\text{prlink}}L) \mu\text{W}$: where L is a length of link (mm) to relay 1 bit of traffic. In this paper, this model is used to evaluate the energy consumption. In our comparison, we first set E^{packet} to 0.98, E^{circuit} to 0.37, E^{stlink} to 0.39, and E^{prlink} to 0.12, according to results by Wolkotte et al. [13]. Then, we also investigate the impact of the ratio of the energy consumption of the packet and circuit switches by changing E^{circuit} .

In this paper, we focus only on the energy consumed by the network, and exclude the energy consumed by the cores, because the energy consumed by the cores is independent from the network structures.

2) *Traffic Model*: According to Benson et al. [10], each server communicates with only a small number of servers



(a) Same layer connection



(b) Different layer connection

Figure 5. Connection from servers

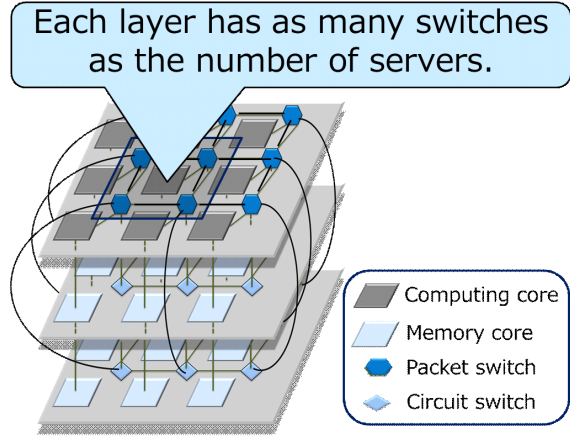
at once, though all server pairs can communicate with each other and communicating server pairs change in time. In this paper, we focus on the energy consumption to relay all traffic generated at a certain time period. Thus, we generate traffic between the server pairs selected by using the uniform random values, and set the traffic rates between the server pair to 10,000 bits. In our evaluation, we vary the number of communicating server pairs from 500 to 2,000, and generate 10 patterns of traffic for each of the cases of the number of communicating server pairs by using the different random seeds.

3) *Latency Model*: In this paper, we also compare the latency to relay the generated traffic. We define the latency as the time required to receive all traffic by the destination servers after generating the traffic demands.

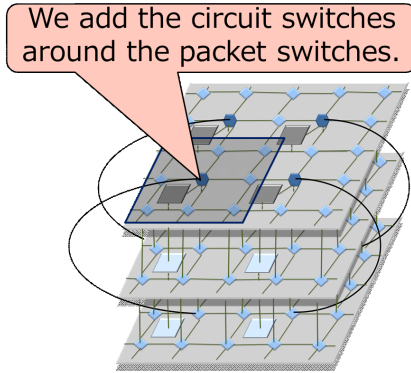
In this paper, we assume that each packet can be relayed by a packet switch to the next packet switch in 1 clock cycle. Though the clock cycle required to relay a packet depends on the switch architectures and may be different from this model. The suitable network structures discussed in this paper are independent of switch architectures because the order of latencies is the same as the results in this paper even if multiple clock cycles are required to relay a packet.

In the on-chip data center, we also use the circuit switches. The circuit switch is configured to connect the input and output ports in advance. The packet switches can be connected by configuring the circuit switches. The packet switch pairs, connected by the circuit paths, relay the packets by the same way as the packet switches that are directly connected to each other. The relay of the packets by the circuit switch takes no clock cycles. Thus, the latency depends only on the number of packet switches passed by the flow.

4) *Path Computation Model*: We calculate the routes of traffic so as to make the energy consumed by the traffic small. In this paper, the route of each traffic demand is calculated by the Dijkstra algorithm setting the weights of the links to the



(a) Minimum placement



(b) Additional circuit switch placement

Figure 6. Placement of switches within each layer

energy consumed to relay the traffic. If the calculated route uses the circuit switch, we connect both ends of the input and the output ports, and remove the ports of the circuit switch before the calculation of the routes of the next traffic demands, so as to avoid the output ports of the circuit switch used by the other traffic from the different input ports.

In this path computation, we assume that the traffic demands are known before calculating the routes. By using this model, we discuss the suitable network structure when the routes are calculated optimally. However, the actual traffic demands may be unknown when calculating routes, and we require a method to calculate the routes without traffic demand information, which is one of our future work.

C. Network Structure Suitable to On-Chip Data Centers

In this subsection, we discuss the network structure suitable to on-chip data centers, which accommodates traffic between servers with low energy consumption. We compare the network structures constructed by various parameters of the network structures. The network structure has three kinds of parameters as described in Section III-A. For each kind of parameter, we have two types of settings. Therefore, $2 \times 2 \times 2 = 8$ network structures are constructed by setting the parameters of the network structure. In this subsection, we compare all of them.

To evaluate the energy consumption, we use the energy model based on the results by Wolkotte et al. [13]. That is,

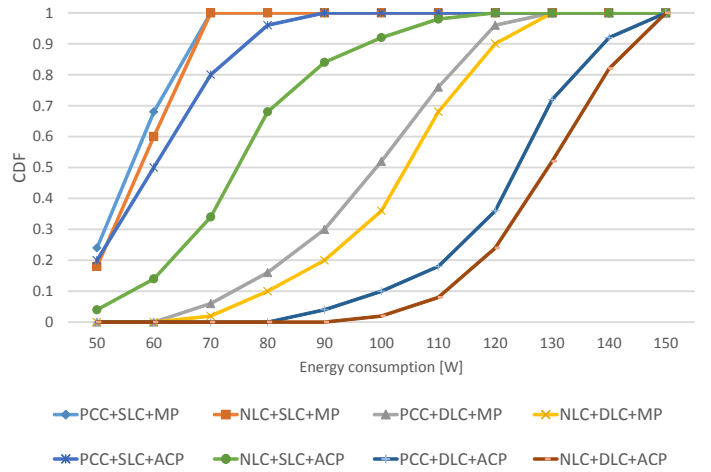


Figure 7. CDF of the energy consumption (Chip size= 10×10 , Number of communicating server pairs=1000, Energy model by Wolkotte et al. [13])

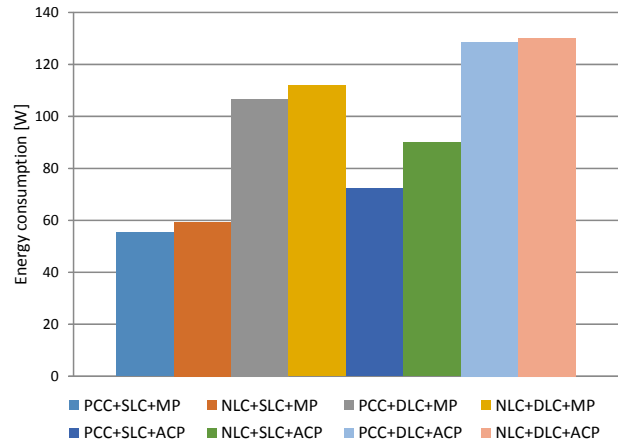


Figure 8. Comparison of the worst-case energy consumption (Chip size= 10×10 , Number of communicating server pairs=1000, Energy model by Wolkotte et al. [13])

we set E^{packet} to 0.98, E^{circuit} to 0.37, E^{stlink} to 0.39, and E^{prlink} to 0.12. We set the number of servers in the chip to 100, and the servers are placed in 10×10 lattice. We set the length of the intra-layer link to 2 mm, and the length of the inter-layer link to $1 \mu\text{m}$. We select 1000 communicating server pairs randomly and generate traffic between the selected server pairs.

Figure 7 shows the comparison of the cumulative distribution function of the energy consumption. The vertical axis is the cumulative distributed function, and the horizontal axis is the energy consumption. We also compare the worst-case energy consumption, and the average of the energy consumption in Figures 8 and 9. In these figures, the vertical axis is the energy consumption.

Figure 10 shows the comparison of the cumulative distribution function of the latency. The vertical axis is the cumulative distribution function, and the horizontal axis is the latency. We also compare the worst-case of the latency in Figure 11.

The rest of this subsection discusses the impact of each parameter of the network structure.

1) *Comparison of Inter-layer connections:* We first discuss the impact of the inter-layer connections by comparing the

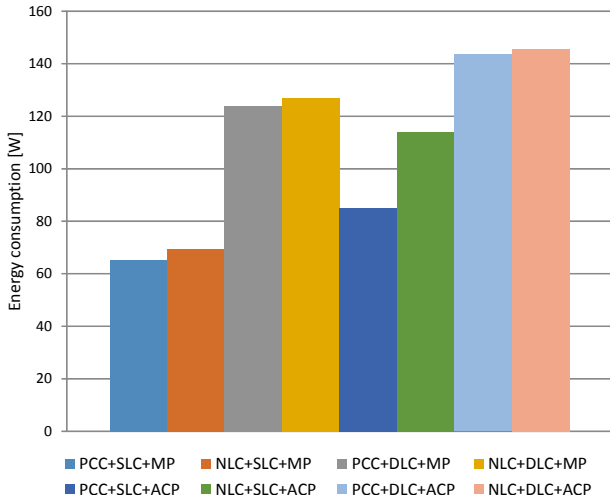


Figure 9. Comparison of the average of the energy consumption (Chip size= 10×10 , Number of communicating server pairs=1000, Energy model by Wolkotte et al. [13])

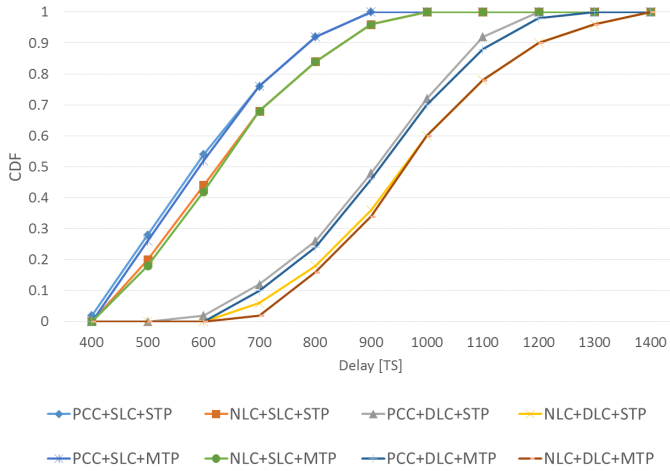


Figure 10. CDF of the latency (Chip size= 10×10 , Number of communicating server pairs=1000, Energy model by Wolkotte et al. [13])

network structures with the PCC and those with the NLC. That is, we perform the following comparisons.

- Network structure with PCC, SLC and MP vs. Network structure with NLC, SLC and MP
- Network structure with PCC, DLC and MP vs. Network structure with NLC, DLC and MP
- Network structure with PCC, SLC and MP vs. Network structure with NLC, SLC and ACP
- Network structure with PCC, DLC and MP vs. Network structure with NLC, DLC and ACP

Figures 7, 8, and 9 show that the energy consumption of the network structures with the PCC is always smaller than those with the NLC. This is because a circuit path using the circuit switch whose layer is far from the packet switch is required to pass multiple layers in the NLC as shown in Figure 12. Because each circuit switch relaying the traffic consumes energy, the large number of circuit switches passed by the circuit paths causes a large energy consumption. On the

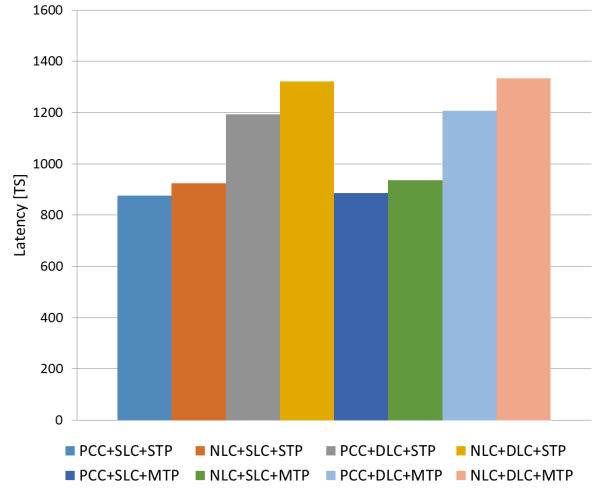


Figure 11. Comparison of the worst-case of the latency (Chip size= 10×10 , Number of communicating server pairs=1000, Energy model by Wolkotte et al. [13])

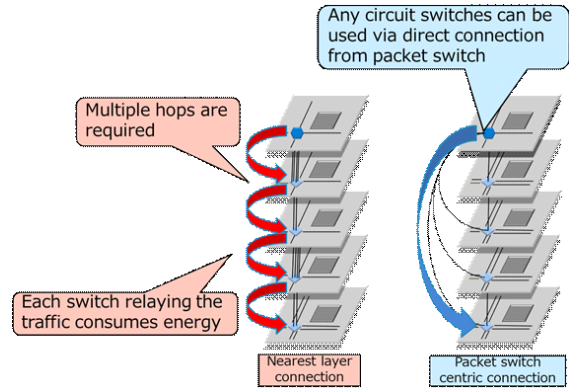


Figure 12. The cause of the difference between the PCC and the NLC

other hand, the packet switches are directly connected to the circuit switches in all layers in the PCC, and the number of switches passed by traffic is smaller than the NLC.

Figures 10 and 11 show that the PCC also achieves smaller latency than the NLC. This is because the PCC establishes more circuit paths since circuit paths consumes less energy in the network structures with the PCC than the NLC. The circuit paths reduce not only the energy consumption but also the latency, because the packet switch relays the packet to the switch connected via the circuit path within one clock cycle.

2) *Comparison of the Connection between Servers and Switches:* We investigate the impact of the connection between servers and switches by comparing the network structures with the SLC and those with the DLC. That is, we perform the following comparisons.

- Network structure with PCC, SLC and MP vs. Network structure with PCC, DLC and MP
- Network structure with NLC, SLC and MP vs. Network structure with NLC, DLC and MP
- Network structure with PCC, SLC and MP vs. Network structure with PCC, DLC and ACP
- Network structure with NLC, SLC and MP vs. Net-

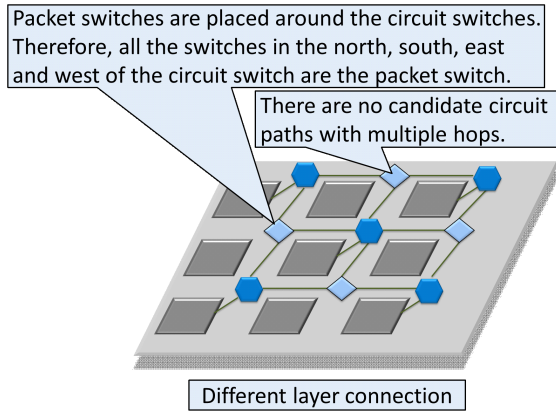


Figure. 13. Circuit path establishment within a layer in the DLC

work structure with NLC, DLC and ACP

Figures 7, 8, and 9 show that the energy consumption of the network structures with the SLC is smaller than those with the DLC. There are two reasons for this. The first reason is that the packet switches prevent establishment of long circuit paths in the DLC. As shown in Figure 13, the packet switches are placed around the circuit switches in some layers in the DLC, and the circuit paths with multiple hops should be established via any layers including the circuit switches in the network structure with the SLC.

The other reason is that there are no packet switches directly connected to each other in the DLC. Therefore, even the flow between the servers neighboring with each other requires the circuit paths, which consumes more energy than the directly connected link between packet switches.

Figures 10 and 11 show that the SLC achieves the smaller latency than the DLC, because the SLC can establish more circuit paths than the DLC.

3) Comparison of Placement of Switches within a Layer:

Finally, we discuss the impact of the placement of switches within a layer. The ACP increases the number of candidate routes for the circuit paths. However, the number of hops becomes larger than the MP. Comparing the network structures with the ACP and those with the MP, we clarify whether the larger number of candidate circuit paths is preferable or the smaller number of hops between servers is preferable.

We compare the network structures with the MP and those with the ACP. That is, we perform the following comparisons.

- Network structure with PCC, SLC and MP vs. Network structure with PCC, SLC and ACP
- Network structure with NLC, SLC and MP vs. Network structure with NLC, SLC and ACP
- Network structure with PCC, DLC and MP vs. Network structure with PCC, DLC and ACP
- Network structure with NLC, DLC and MP vs. Network structure with NLC, DLC and ACP

Figures 7, 8, and 9 show that the network structures with the MP always achieve a smaller energy consumption than those with the ACP. That is, in despite of the large number of candidate circuit paths, the ACP does not reduce the energy consumption.

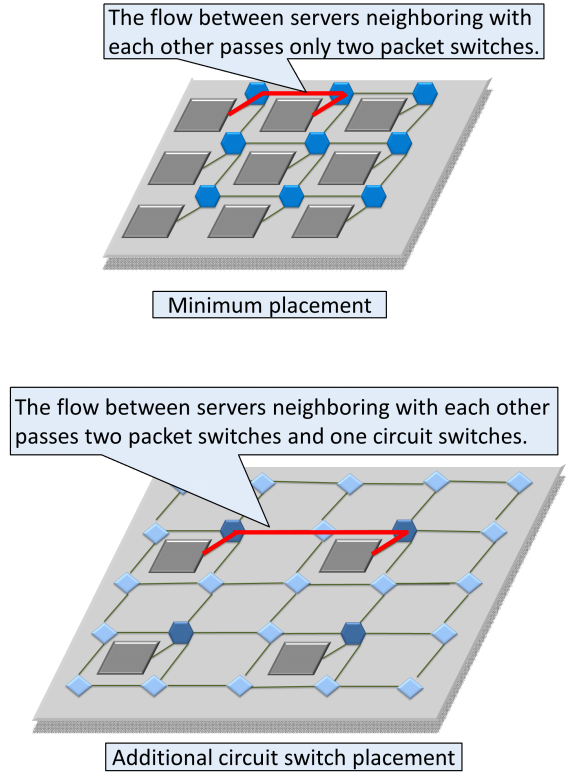


Figure. 14. Routes of the flow between the servers neighboring with each other

This is because a sufficient number of circuit paths are established even in the network structures with the MP. In addition, circuit paths pass more circuit switches in the network structures with the ACP than those with the MP. Especially, the flow between servers neighboring with each other passes only two packet switches in the network with the MP, but it passes two packet switches and one circuit switches in the network with the ACP as shown in Figure 14. Such additional switches passed by the flows increases the energy consumption.

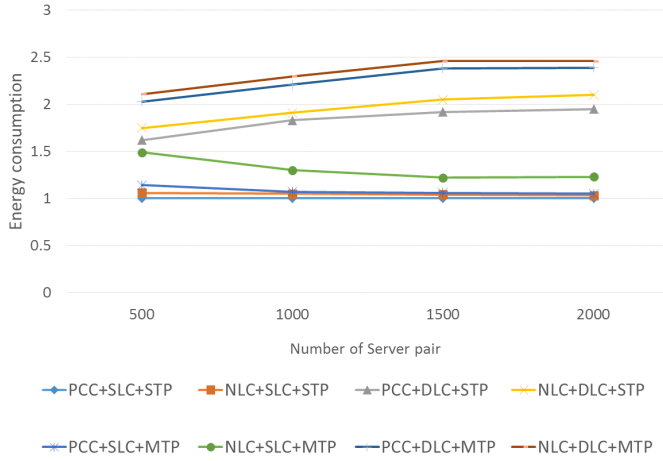
Figures 10 and 11 show that the MP and ACP achieve the similar latency. This is because the similar number of circuit paths are established in the MP and the ACP as discussed above.

4) Summary of the Results: As discussed above, to save the energy consumption and reduce the latency, (1) the suitable inter-layer connection is the PCC, (2) the suitable connection between servers and switches is the SLC, and (3) the suitable placement of switches within a layer is the MP.

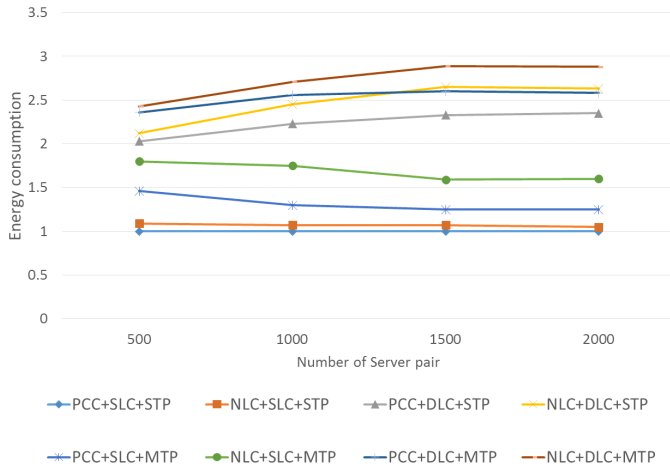
D. Impact of the number of communicating server pairs

In Section III-C, we investigated only the case that the number of communicating server pairs is 1000. However, the number of communicating server pair has an impact on the energy consumption or the latency of the network; as the number of communicating server pair increases, the energy consumption becomes large. This may have an impact on the suitable network structures.

In this subsection, we discuss the impact of the number of communicating server pairs on the suitable network structures. In this subsection, we compare the network structures, changing the number of communicating server pairs from 500



(a) Average



(b) Worst-case

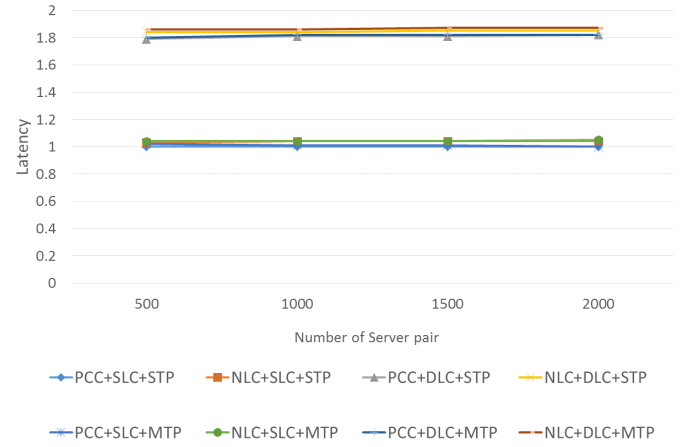
Figure 15. The impact of the number of communicating server pairs on the energy consumption

to 2,000. We set the other parameters to the same values as Section III-C. We generated 10 patterns of traffic for each case.

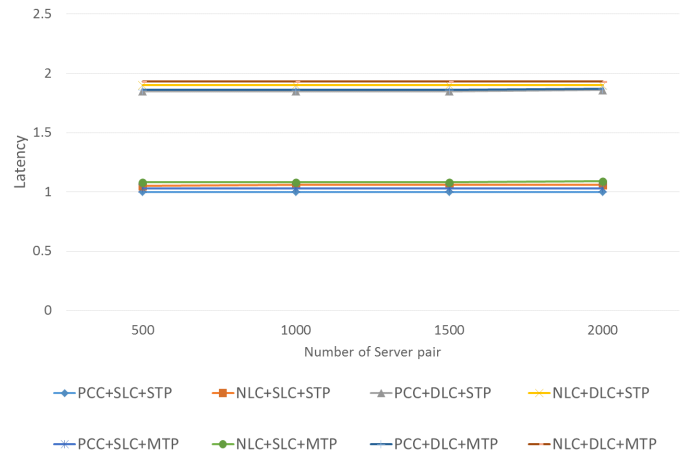
Figures 15 and 16 show the results. In these figures, the horizontal axis is the number of communicating server pairs, and the vertical axis is the energy consumption or latency normalized by that of the network structure with the PCC, the SLC and the MP, that achieves the smallest energy consumption in the results.

As shown in Figure 16, the number of communicating server pairs has no impact on the ratio of the latency of the network structures. The latency depends on the number of packet switches passed by each packet. The number of packet switches passed by each packet depends on whether the circuit paths to bypass packet switches can be established, and is independent from the number of communicating server pairs. As a result, the number of communicating server pairs has no impact on the ratio of the latency. Therefore, the rest of this subsection discusses the impact of the number of communicating server pairs on the energy consumption.

1) *Impact on Suitable Inter-layer Connections*: First, we investigate the impact of the number of communicating server



(a) Average



(b) Worst-case

Figure 16. The impact of the number of communicating server pairs on the latency

pairs on the suitable inter-layer connections.

Figure 15 shows that the network structures with the PCC consume the smaller energy than those with the NLC regardless of the number of communicating server pairs. As discussed in Section III-C1, the difference of the energy consumption between the PCC and the NLC is caused by the difference of the number of switches passed by the circuit paths. Regardless of the number of communicating server pairs, the number of switches passed by the circuit paths in the NLC is larger than those in the PCC, because the circuit paths pass multiple layers to use the circuit switches in the layer far from the packet switch in the NLC while each packet switch has direct connection to any layers in the PCC. As a result, even if the communicating server pair changes, the network structures with the PCC achieves the small energy consumption.

2) *Impact on Suitable Connection between Servers and Switches*: We investigate the impact of the number of communicating server pairs on the suitable connection between servers and switches.

Figure 15 shows that the energy consumption of the network structures with the DLC is larger than those with the SLC, and the difference of the energy consumption increases

as the number of communicating server pair increases. As discussed in Section III-C2, one of the reasons of the difference of the energy consumption between the SLC and the DLC is the difference of the number of candidate circuit paths. When the number of communicating server pairs is large, a large number of circuit paths are established to accommodate the flows between server pairs with a small energy consumption in the network structures with the SLC. However, due to the small number of candidate circuit paths, in the network structures with the DLC, we cannot establish as many circuit paths as the SLC. As a result, the difference of the number of established circuit paths causes the difference of the amount of traffic passing the packet switches; more traffic passes the packet switches and consumes more energy in the network structures with the DLC than those with the SLC.

3) *Impact on Suitable Placement of Switches within a Layer:* Finally, we investigate the impact of the number of communicating server pairs on the suitable placement of switches within a layer.

Figure 15 shows that the energy consumption of the network structures with the ACP is larger than those with the MP, but the difference of the energy consumption decreases as the number of communicating server pair increases.

The difference of the energy consumption between the network structures with the MP and those with the ACP is caused by the difference in the number of candidate circuit paths and the length of the circuit paths; the network structures with the ACP provides more candidate circuit paths than the network structures with the MP, though the number of circuit switches passed by the circuit paths is large. When the number of communicating server pairs is small, both of the MP and the ACP can establish the sufficient number of circuit paths. Thus, the difference of the energy consumption is caused only by the difference of the number of switches passed by the circuit paths, and the network structures with the MP achieve the smaller energy consumption than the ACP. On the other hand, when the number of communicating server pairs is large, more circuit paths are required. In this case, the MP cannot establish the sufficient number of circuit paths, and the flows passes multiple packet switches. In the ACP, we add more circuit paths, though the number of circuit switches passed by the circuit paths is large. This causes the decrease of the difference of the energy consumption between the MP and the ACP.

Figure 15 shows that even when the number of communicating server pairs is 2,000, the network structures with the MP achieve the smaller energy consumption than those with the ACP. When the number of communicating server pairs is 2,000, each server communicates with 20 % of the servers at once. Because each server communicates with only a small number of servers at once in the typical data centers [10], the case that each server communicates with more than 20 % of the servers seldom occurs. Therefore, the MP is suitable for the on-chip data centers regardless of the number of communicating server pairs.

E. Impact of the size of the chip

In the above discussions, we investigate only the case that the chip includes 100 servers. However, the size of the chip has an impact on the energy consumption of the network; as the size of the chip increases, the energy consumption becomes large. This may have an impact on the suitable

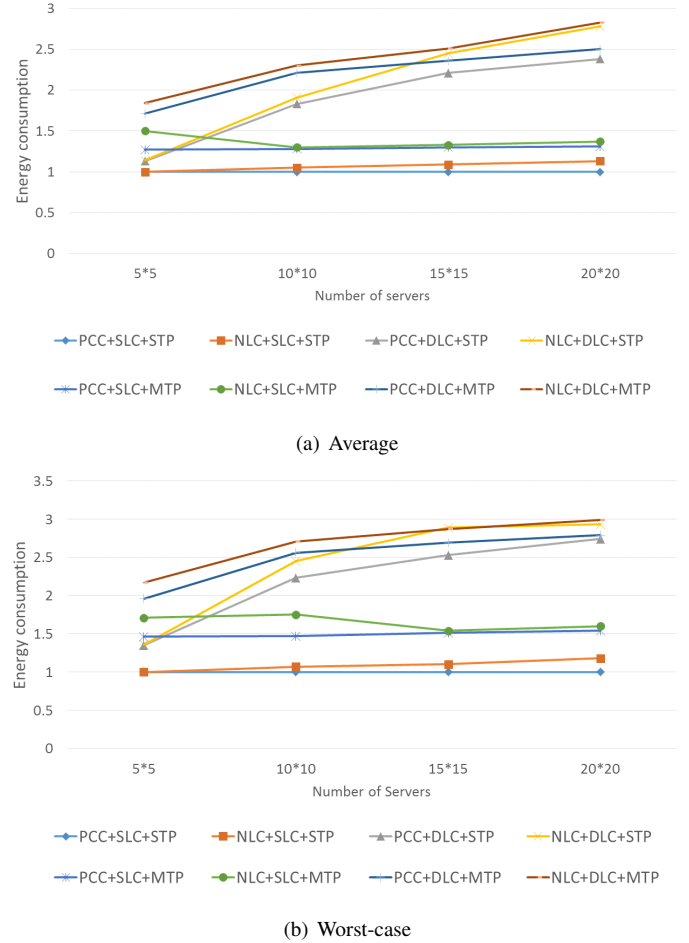


Figure 17. Impact of the size of the chip on the energy consumption

network structure.

In this subsection, we discuss the impact of the size of the chip on the suitable network structures. In this subsection, we compare the network structures, changing the number of servers within a chip from 25 to 400. We set the other parameters to the same values as Section III-C.

Figures 17 and 18 show the results. In these figures, the horizontal axis is the size of the chip, and the vertical axis is the energy consumption or latency normalized by that of the network structure with the PCC, the SLC and the MP, that achieves the smallest energy consumption in results.

Based on these figures, the rest of this subsection discusses the impact of the size of the chip on suitable parameters of the network structures.

1) *Impact on Suitable Inter-layer connections:* We discuss the impact of the size of the chip on the suitable inter-layer connections.

Figure 17 shows that the energy consumption of the network structures with the PCC is smaller than those with the NLC regardless of the size of the chip, though there are the cases that the difference is significantly small.

As discussed in Section III-C1, the difference of the energy consumption between the PCC and the NLC is caused by the difference of the number of switches passed by the circuit paths. If we can establish the sufficient number of circuit paths without using the layers far from the packet switches, the

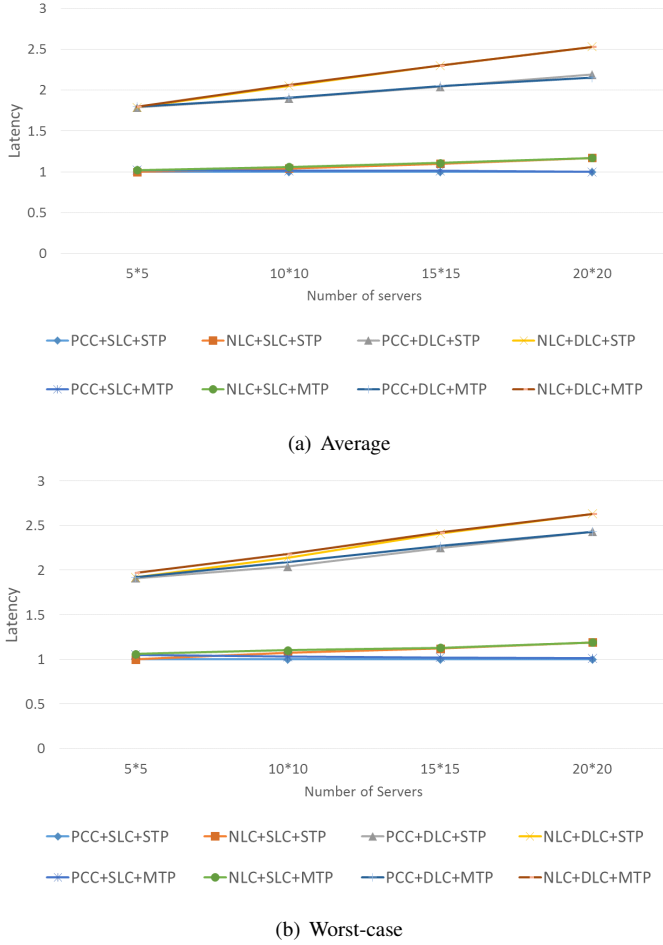


Figure 18. Impact of the size of the chip on the latency

network structures with the NLC achieves the similar energy consumption to those with the PCC. However, the number of circuit switches passed by the circuit paths in the network structures with the NLC is always larger than those with the PCC, because the circuit paths passes multiple layers to use the circuit switches in the layer far from the packet switch in the NLC while each packet switch has direct connection to any layers in the PCC. As a result, the energy consumption of the network structures with the PCC is smaller than those with the NLC regardless of the size of the chip.

Figure 18 shows that the latency of the network structure with the PCC is smaller than those with the NLC, and the difference becomes large as the size of the chip increases. This is because the PCC tends to establish more circuit paths than the NLC, because establishing the circuit paths in the PCC consumes less energy than the NLC. As the size of the chip increases, the number of hops of the established circuit paths becomes large, and the latency reduced by establishing the circuit path becomes large. As a result, the difference of the latency caused by the difference of the number of the established circuit paths becomes large as the size of the chip increases.

2) *Impact on Suitable Connection between Servers and Switches:* We investigate the impact of the size of the chip on the suitable connection between servers and switches.

Figure 17 shows that the energy consumption of the

network structures with the SLC is smaller than those with the DLC, and the difference becomes large as the size of the chip increases. As the size of the chip becomes large, the difference of the energy consumption between the circuit paths and the routes without using the circuit paths becomes large, due to the increase of the switches passed by the flow. Thus, more circuit paths are required to be established. However, the number of candidate circuit paths in the network structures with the DLC is smaller than that in the network structures with the SLC. Thus, we cannot establish the sufficient number of circuit paths in the DLC because of the lack of the candidate paths, while sufficient number of circuit paths are established in the SLC. This causes the increase of the difference of the energy consumption.

Figure 18 shows that the latency of the network structures with the SLC is smaller than those with the DLC and the difference becomes large as the size of the chip increases. This is because we cannot establish the sufficient number of circuit paths in the DLC, while the SLC establishes more circuit paths. As discussed in the section III-E1, the difference of the latency caused by the number of established circuit paths becomes large as the size of the chip. As a result, the difference of the latency between the SLC and the DLC becomes large as the size of the chip increases.

3) *Impact of Suitable Placement of Switches within a Layer:* We discuss the impact of the size of the chip on the suitable placement of switches within a layer.

Figure 17 shows that the energy consumption of the network structures with the MP is smaller than those with the ACP regardless of the size of the chip. This is because even the network structures with the MP have a sufficient number of candidate circuit paths regardless of the size of the chip, though the network structures with the ACP provides more candidate circuit paths than the network structures with the MP. As a result, the ACP consume more energy since the circuit paths pass more circuit switches.

Figure 18 shows that the MP and the ACP achieve the similar latency. This is because the MP and the ACP establishes the similar number of circuit paths regardless of the size of the chip.

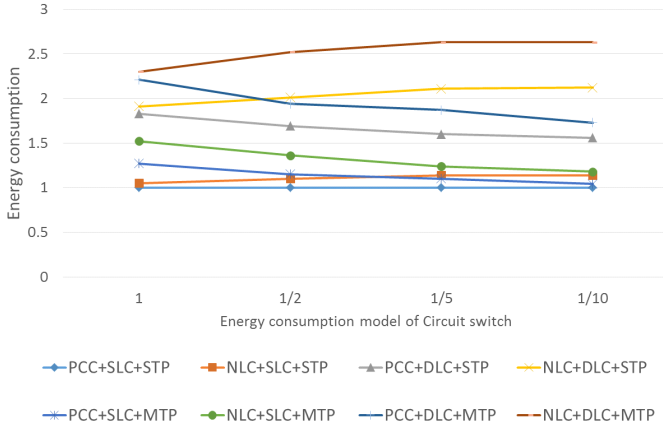
F. Impact of the energy consumption of the switches

In the above discussions, we investigate only the case that the energy consumption of the circuit switch $0.37\mu\text{W/bit}$. However, the energy consumption of the circuit switch depends on the architecture of the switches. Therefore, in this subsection, we investigate the impact of the energy consumption of the switches on the energy consumption of the network structures. We change the energy consumption of the circuit switch from 1/2 to 1/10 of the model used in the previous subsections. We set the other parameters to the same values as Section III-C.

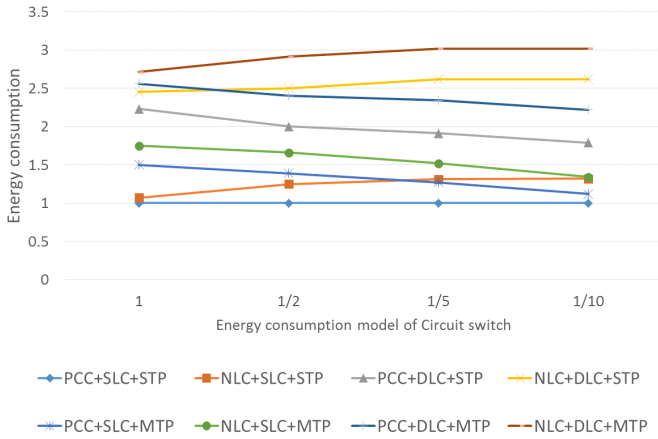
Figure 19 shows the result. In this figure, the horizontal axis is the ratio of the energy consumption of the circuit switch compared with the model by Wolkotte et al. [13], and the vertical axis is the energy consumption normalized by that of the network structure with the PCC, the SLC, and the MP, that achieves the smallest energy consumption in the results.

1) *Impact on Suitable Inter-layer connections:* We investigate the impact of the energy consumption of the circuit switches on the suitable inter-layer connection.

Figure 19 shows that the energy consumption of the network structures with PCC is smaller than those with the NLC,



(a) Average



(b) Worst-case

Figure 19. Impact of the energy consumption of circuit switches on the energy consumption

but the difference becomes small as the energy consumption of the circuit switch decreases. As discussed in Section III-C1, in the NLC, the circuit path passes multiple circuit switches to use the circuit switches in the layer far from the packet switches. Thus, the energy consumption in the case of using the circuit paths is large in the network structure with the NLC, compared with the PCC. When the energy consumption of the circuit switches becomes small, more circuit paths are established because the energy reduction by using the circuit path increases. Thus, the difference caused by the number of circuit switches passed by the circuit paths becomes large.

2) *Impact on Suitable Connection between Servers and Switches:* In this subsection, we compare the network structures of the different types of the connections between servers and switches.

Figure 19 shows that the energy consumption of the network structures with the SLC is smaller than those with the DLC, and the difference becomes small as the energy consumption of the circuit switch becomes small except the comparison between the network structure with the NLC, the SLC and the ACP, and that with the NLC, the DLC and the ACP, where the number of the circuit switches passed by the circuit paths is the largest among the compared network

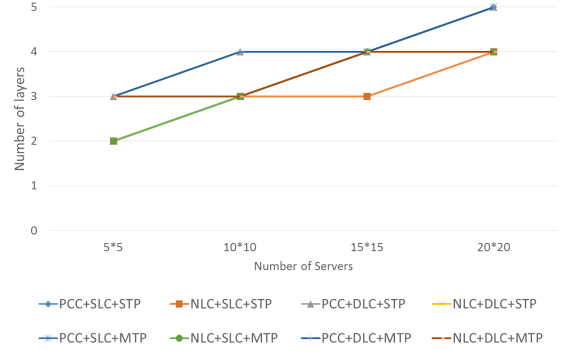


Figure 20. The cause of the difference between the PCC and the NLC

structures. As discussed in Section III-C2, the circuit paths is required even for the flow between the servers neighboring with each other in the DLC, which is one of the reasons why the DLC consumes more energy than the SLC. As the energy consumption of the circuit switches becomes small, the energy consumed by the circuit paths established for the flows between the servers neighboring with each other decreases. As a result, the difference of the energy consumption between the SLC and the DLC becomes small.

However, as shown in Figure 19, even if the energy consumption of the circuit switch becomes 1/10 of the model by Wolkotte et al. [13], the energy consumption of the network structures with the DLC is much larger than those with the SLC. That is, even if the energy consumption of the circuit switches is reduced, the SLC is suitable to the on-chip data centers.

3) *Impact on Suitable Placement of Switches within a Layer:* Finally, we compare the impact of the energy consumption of circuit switches on the suitable placement of switches within a layer.

Figure 19 shows that the energy consumption of the MP is smaller than the ACP, but the difference becomes small as the energy consumption of the circuit switch becomes small. This is because the network structures with the ACP has more candidate circuit paths between packet switches, though the number of circuit switches passed by the circuit paths is large. As the energy consumption of the circuit switch becomes small, the additional energy caused by the number of circuit switches passed by the circuit paths becomes small, and the impact of the number of candidate circuit paths becomes large.

However, even when the energy consumption of the circuit switches becomes 1/10 of the model by Wolkotte et al. [13], the ACP consumes more energy than the MP. That is, even if the energy consumption of the circuit switches is reduced, the MP is suitable to the on-chip data centers.

G. The number of the required layers

In the network structure with the PCC, SLC, and STP, the circuit switch nearest to the packet switch among the available circuit switches is used to establish a circuit path, because using the circuit paths far from the packet switch consumes more energy. Thus, even if we construct an on-chip data center with many layers, the layers far from the packet switches may not be used at all.

In this subsection, we investigate the number of layers used to establish a circuit switches. Figure 20 shows the results. In

this figure, the horizontal axis is the size of the chip, and the vertical axis is the maximum number of layers used to establish circuit paths in our method.

As shown in Figure 20, as the number of servers increases, the number of used layers becomes large. However, Figure 20 indicates that the circuit switches at the 5-th layer are never used even in case of 15*15 servers. That is, a small number of layers is sufficient in the on-chip data center.

IV. CONCLUSION AND FUTURE WORK

In this paper, we evaluated the 3D on-chip network structures for the on-chip data centers, which uses both of the circuit and packet switches. According to the results, to reduce the energy consumption, (1) the servers should connect to the packet switches in the same layer, (2) the packet switches should connect to the circuit switches in all layers, and (3) each layer should include minimum number of switches, regardless of the size of the chip, and the ratio of the energy consumption of the packet and circuit switches.

Our future work includes the method to calculate the routes suitable to the on-chip networks.

ACKNOWLEDGMENTS

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REFERENCES

- [1] T. Ikeda, Y. Ohsita and M. Murata, "3D on-chip data center networks using circuit switches and packet switches," in *Proceedings of The Eighth International Conference on Systems and Networks Communications*, Oct. 2013, pp. 125–130.
- [2] D. Abts and B. Felderman, "A guided tour of data-center networking," in *Communications of the ACM*, vol. 10, Jun. 2012, pp. 44–51.
- [3] J. G. Koomey and P. D., "Growth in data center electricity use 2005 to 2010," *The New York Times*, Aug. 2011.
- [4] R. Iyer, R. Illikkal, L. Zhao, S. Makineni, D. Newell, J. Moses, and P. Apparao, "Datacenter-on-chip architectures: Tera-scale opportunities and challenges in Intel's manufacturing environment," in *Intel Technology Journal*, vol. 11, Aug. 2007, pp. 227–237.
- [5] M. Kas, "Toward on-chip datacenters: a perspective on general trends and on-chip particulars," in *The Journal of Supercomputing*, vol. 62, Oct. 2012, pp. 214–226.
- [6] T. Bjerregaard and S. Mahadevan, "A survey of research and practice of network-on-chip," vol. 1-51, Mar. 2006.
- [7] A. Ankur, C. Iskander, and R. Shankar, "Survey of network on chip architectures & contributions," *Journal of Engineering, Computing and Architecture*, pp. 21–27, 2009.
- [8] M. B. Stensgaard and J. Sparso, "ReNoC: A network-on-chip architecture with reconfigurable topology," in *Proceedings of the Second ACM/IEEE International Symposium on Networks-on-Chip*, Apr. 2008, pp. 55–64.
- [9] M. Modarressi, H. Sarbazi-Azad, and M. Arjomand, "A hybrid packet-circuit switched on-chip network based on sdm," in *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition, 2009. DATE '09*, Apr. 2009, pp. 566–569.
- [10] T. Benson, A. Anand, A. Akella, and M. Zhang, "MicroTE : Fine grained traffic engineering for data centers," in *Proceedings of the Seventh Conference on emerging Networking EXperiments and Technologies*, Dec. 2011, pp. 1–12.
- [11] J. Dean and S. Ghemawat, "MapReduce: simplified data processing on large clusters," in *Communications of the ACM*, vol. 51, Jan. 2008, pp. 107–114.
- [12] J. Leibusky, G. Eisbruch, and D. Simonassi, "Getting Started with Storm," in *O'Reilly*, 2012.
- [13] P. T. Wolkotte, G. J. M. Smit, N. Kavaldjiev, J. E. Becker, and J. Becker, "Energy model of networks-on-chip and a bus," in *Proceedings of IEEE International Symposium on System-on-Chip*, Nov. 2005, pp. 82–85.