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パケット保持時間に制約がある光RAMバッファの導入による全光パケットスイッチの性能改善効果

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あらまし　光パケットスイッチにおいて生じるパケット競合を解消する手段として，波長変換による波長上の競合回避や固定遅延を与えるファイバ遅延線による時間軸上の競合回避が検討されてきた．近年は，ナノ加工技術の進展により，電気処理することなく光信号を保持する光 RAM デバイスの研究開発が進展しつつある．特に，フォトニック結晶を用いた光 RAM デバイスは高度な集積化が可能とされており，光パケットスイッチのバッファシステムへの適用が期待される．ところが，フォトニック結晶を用いた光 RAM デバイス固有の課題として，動作波長への依存性やビット情報の保持時間などの技術的制約が考えられる．本稿では，フォトニック結晶を用いた光 RAM デバイスおよびバッファシステムを対象とし，光 RAM バッファを導入する性能改善効果を明らかにするとともに，光パケットスイッチに適用する場合に求められる性能要件を明らかにする．計算機シミュレーションによる評価の結果，8×8，波長多重数 8，かつ，波長当たりの回線容量が 40Gbps の共有バッファ型光パケットスイッチにおいて，15 パケット程度のバッファ容量と 200ns 程度の保持時間が必要となることが明らかとなった．

キーワード　光パケットスイッチ，共有バッファ型，光 RAM，競合回避，保持時間

Benefits of Optical RAM Buffer in All-optical Packet Switch

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Abstract　Optical RAM buffer is vital devices for the optical packet switching. In this paper, we investigate the benefit of optical RAM buffer that employs an optical bistable device. The photonic crystal cavity realizes strong light confinement, and expected to realize an integrated one-chip all-optical memory. We evaluate the packet loss probability of optical packet switches by incorporating three characteristics introduced by the optical bistable device; size of buffer, wavelength dependency, and packet lifetime. The results show that the benefit of optical RAM buffer is significant when the offered load is low and when the number of buffering port is enough. We also investigate the impact of packet lifetime on the packet loss probability. The results show that InGaAsP-based photonic crystal cavities demonstrated in the recent paper certainly improve the packet loss probability, however, extending the packet lifetime from 150 ns to 200ns will improve the packet loss probability significantly.

Key words　Optical packet switching, shared buffering, optical RAM, contention resolution, photon lifetime

1. Introduction

Recent advances in optical technologies such as wavelength division multiplexing (WDM) have allowed us to achieve ultra-high data-transmission in optical networks. WDM technology offers multiple wavelengths on a single fiber, which drastically increases the bandwidth of links between nodes. However, increasing the link bandwidth only does not resolve the network bottleneck sufficiently because of a limitation of packet processing capacity at nodes.

Various approaches have been investigated to overcome the limitation of packet processing capacity of nodes. Among them, optical packet switching (OPS) that switches the packet with no electronic processing is expected to overcome the limitation, while bringing the flexibility and efficiency of the Internet to optical networks.

One of the difficulties of OPS networks is buffering optical packets in the network. In electronic packet switched network, contention of packets is resolved by storing the contended packets in random access memory (RAM) and sending out the packets with reading operation when the output port is free. However, the operation is difficult in the optical domain, because there is no equivalent optical RAM available for storing packets. Converting packets from optical domain to electronic domain in order to use electronic RAM is not a feasible solution because of the processing overheads of electronic RAM. Current electronic devices are not fast enough to process the data at the ultra high speed of optical networks.

Contention resolution by using fiber delay lines (FDLs) where packets are delayed by a fixed amount of time through optical fibers have been investigated in literatures [1]. However, physical impairments of optical packets occur when we deploy the FDLs as a buffering system, since packets must traverse delay lines. Furthermore, due to the fixed delay of FDLs, scheduling the departure time of contended packets requires high computational complexity, which will become significant as the size of optical packet switch and/or transmission capacity increases. More importantly, an upper-layer protocol such as TCP uses the order of packets as a sign of congestion in a network. That is, fixed delay by buffering system may cause the out-of-order packets, which in turn leads to severe throughput degradation for the upper-layer protocol. Therefore, the optical RAM that can read the packet whenever the output port becomes free is important for the optical packet switching.

Recently, an optical bistable device by using silicon-based photonic crystal cavities has demonstrated in Ref. [2]. The photonic crystal cavity realizes strong light confinement, and expected to realize an integrated one-chip all-optical memory. A cavity in the device resonates at two different wavelength; one for $\lambda_c = 1536.47$nm, another for $\lambda_s = 1569.70$nm. By injecting set/reset pulses to the cavity, one-bit information can be stored. An optical RAM buffer system using the optical bistable devices is suggested in Refs. [3–5].

However, there are several technical constraints on the optical RAM buffer. First, comparing with the electronic memory where highly sophisticated integrated-circuit technology is deployed, the capacity of high-speed, lower-energy optical RAM buffer is small. Second, operating wavelengths of the optical bistable device is restricted. That is, wavelength conversion from WDM's telecommunication wavelengths to the operating wavelength is necessary to store contended optical packets. Since the wavelength conversion can be used for the contention resolution [6], there are always two contention resolution schemes in optical packet switch that deploys the optical RAM buffer. An effectiveness of buffering functionality in addition to the wavelength conversion should be clarified, which is our primal concern in this paper. Lastly, holding time of the all-optical bistable memory is limited due to accumulated heat in the cavity. In the case of Si-based photonic crystal cavity demonstrated in Ref. [2], the memory holding time is limited to less than 2.5ns, which means that packet contention can be resolved only when the overlapped region is less than 100 bits (assuming 40Gbps line-speed). Further development shows that InGaAsP-based photonic crystal achieves 150 ns of memory holding time with 250 μw for the bias power [7].

In this paper, we evaluate the packet loss performance of optical packet switches that deploys the optical RAM buffer system. Since the optical bistable device has several technical constrains as mentioned above, we address 1) how much buffer do we need, 2) how long should the memory holding time be, and 3) how much improvement can we expect by the optical RAM buffer system.

This paper is organized as follows. In Section 2., we show the optical packet switch architecture evaluated in the paper and explain the optical RAM buffer system. Section gives simulation results and discussions. Finally, we conclude this paper in Section 4.

2. Optical Packet Switch Architecture

2.1 Optical packet switch with optical RAM buffer system

Our optical packet switch architecture used in this paper is shown in Figure 1. The optical packet switch is equipped with wavelength converters and optical RAM buffers that resolve packet contentions in a wavelength domain and a time domain respectively. W wavelengths are multiplexed on the fiber and optical packets are carried from each wavelength.

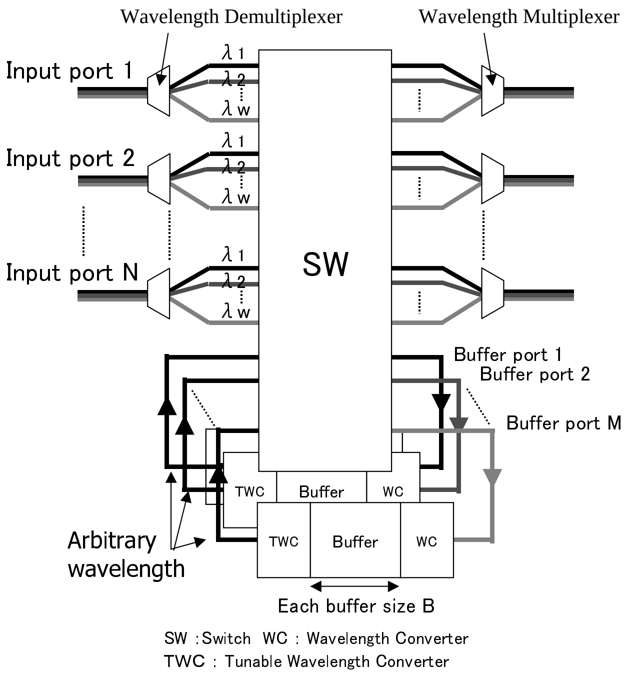

Figure 1 Optical packet switch with optical RAM buffer system

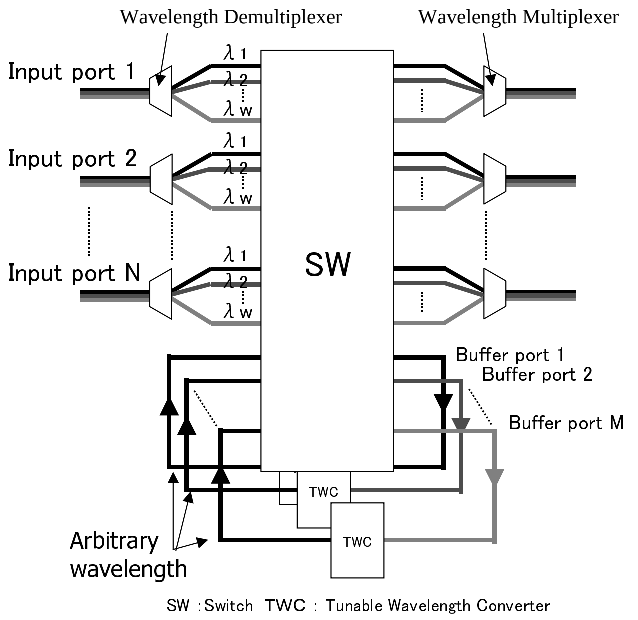

Figure 2 Optical packet switch without using optical RAM buffer system

For the contention resolution purpose, the optical packet switch has M optical RAM buffers, each of which stores B bytes packets, are shared in the optical packet switch. The wavelength converter is placed at the input and output ports of optical RAM buffer. This is because the wavelength dependency of the cavity resonance used in the optical bistable device. Tunable wavelength converter converts from the operating wavelength to the wavelength of WDM transmission channel, and wavelength converter converts from the wavelength of WDM transmission channel to the operating wavelength.

Each incoming optical packet is first demultiplexed at the input port of optical packet switch. Then, header of the packet is looked up and a packet scheduler determines an appropriate output port. When the packet's wavelength of the corresponding output port is available, the packet is sent to the output port directly with no wavelength conversion. When two or more packets to the same wavelength of the same output port arrive at the same time, the contention of the packet occurred. When the packet contention occurred, one packet is switched to the desired output port and the others are switched to the buffering ports.

At the input port of optical RAM buffer system, the optical packet is converted into an operating wavelength of optical RAM. Then, depending on whether the packet contention can be resolved by waiting at buffer or not, the optical RAM buffer system takes a different behavior. When the wavelength conversion is enough for the contention resolution, the contended packet is immediately sent to the output port of optical RAM buffer system. Since the contended packet uses the operating wavelength inside the optical RAM buffer system, the wavelength conversion from the operating wavelength to a proper wavelength is necessary at the output port. After the wavelength conversion, the contended packet is switched to the appropriate output port of the optical packet switch. When the packet contention cannot be resolved by the wavelength conversion, the contended packet is stored at the optical RAM buffer system until any wavelength of the desired output port becomes available. We will explain the write-in and read-out operations at the optical RAM buffer system in Section 2. 3.

With this optical packet switch architecture, The packet loss occurs when the buffering port is fully utilized and when the amount of waiting packets in the buffer exceeds the buffer size B.

2. 2 Optical packet switch without using optical RAM buffer system

Figure 2 shows optical packet switch architecture without using the optical RAM buffer. When the contention of packets occurs, one packet is switched to the desired output port and the others are switched to the port with the TWC. If there are one or more wavelengths that are currently available at the desired output port, the wavelength of contended packet is converted from the current wavelength to a proper wavelength that resolve the packet contention at the desired output port. Otherwise, i.e., when all of wavelengths is already used for transmitting other packets, the contended packets are dropped.

Apparently, the packet drop performance becomes worse

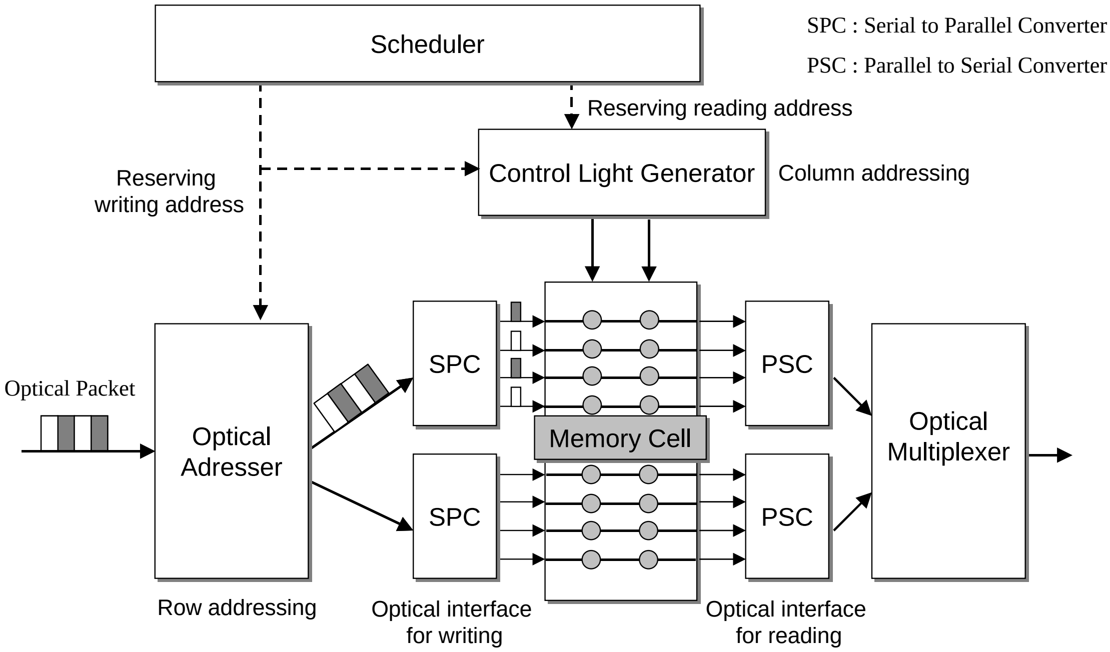

Figure 3 Constitution of optical buffer system using optical memory

with this optical packet switch architecture. However, we will evaluate the packet drop performance in order to investigate effectiveness of buffering functionality in addition to the wavelength conversion functionality.

2. 3 Optical RAM buffer system

In this section, we briefly describe architecture of the optical RAM buffer system, and summarize its characteristic from a viewpoint of networking perspective.

Figure 3 illustrates an optical RAM buffer system that is being developed at Ref. [2, 7, 8]. The optical RAM buffer system mainly consists of four devices; 1) all-optical read-write memory cells, 2) optical addresser, 3) serial/parallel and parallel/serial pulse converters, 4) control light generator used for read-out/write-in light sources. The all-optical read-write memory cells are build on photonic crystal cavities based on a silicon or an InGaAsP. Each cell holds one-bit information in an optical domain through an optical bistable phenomenon [8]. The optical addresser distributes each incoming optical packet to a memory array that is currently available, according to the electronic signal from the buffer scheduler [9]. The serial/parallel pulse converter (SPC) converts the optical packet, which is a serialized optical signal, into optical bit pulses in parallel. In contrast, the parallel/serial pulse converter (PSC) converts optical bit pulses in parallel into a serialized optical signal [10]. The read-out/write-in light sources is used for generating the writing/reading pulses and for a bias light injected into the cavities.

The write operation for the optical packet is as follows. When the packet arrives at the optical RAM buffer system, the scheduler recognizes the arrival of the packet. The buffer scheduler decides memory cells to which the optical signal of input packet is written, according to the current available information on the memory cells. The optical addresser distributes the optical packet to SPC based on the decision of the buffer scheduler. SPC converts serialized optical packet signal to optical bit pulses in parallel. The optical pulses are then propagates to the memory cells. During this, the light sources generate a writing pulse, which activates a cavity in the memory cell, and a bias light to memorize the incoming optical bit pulse. For the reading operation for optical packet, the light source first generates a reading pulse and injected into the cavities. The outputs from cavities are carried to PSC through which optical bit pulses are serialized, and finally leave from the optical RAM buffer system.

2. 4 Characteristics of optical RAM buffer system

Although the optical RAM buffer system achieves asynchronous and burst-mode optical buffering with the order of 100 picoseconds processing speed, there are several technical limitations;

- Size of buffer: Optical bistable operation has been demonstrated by using photonic crystal cavities. Photonic crystal is a promising candidate for the integrated circuit on chips, and an integration of cavities on one-chip will bring the large size of all-optical RAM buffer. However, the circuit integration techniques for the photonic devices are still immature when we compare with integration techniques invested in electronic devices. Thus, the size of all-optical RAM buffer will be smaller than electronic memories such as the high-speed SRAM.

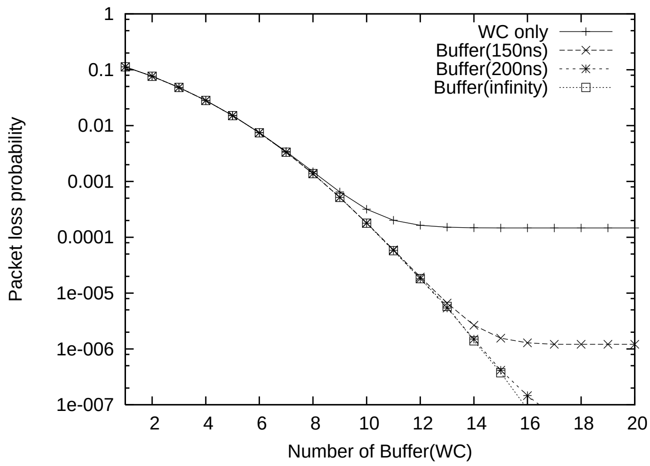

Figure 4 Packet loss probability dependent on the buffer port M

- Wavelength dependency: The optical bistable operation is performed through resonance mode appeared at two different wavelengths. Although the resonance mode depends on the employed devices, wavelengths that can be used for WDM transmission should be converted to operating wavelengths. Since the wavelength conversion can be used for the contention resolution [6], there are always two contention resolution schemes in optical packet switch that deploys the optical RAM buffer.
- Photon lifetime: Holding time of the optical bistable memory is limited due to accumulated heat in the cavity. When the temperature in the resonator rises, memorized information disappears because optical bistable state is canceled in the operating wavelength because of the red-shift in the spectrum. In the case of Si-based photonic crystal cavity, the holding time is limited to less than 2.5ns [2], whereas the InGaAsP-based photonic crystal achieves 150 ns of memory holding time with 250 μw for a bias power [7]. Note that the maximum holding time highly depends on the strength of the bias light, thus the required holding time in optical packet switch should be clarified. From the networking perspective, this characteristic is important in designing the optical packet switch since, unlike the electronic RAM, the optical RAM cannot buffer the optical packet for arbitrary length of time. Hereafter, we call the upper bound of optical packet holding time as *packet lifetime*.

3. Performance Evaluation

3. 1 Simulation model

We conduct computer simulations on optical packet switches depicted in Figs. 1 and 2. As mentioned in Section 2. 4, our optical packet switch that deploys optical RAM buffer system should incorporate three technical constraints; size of buffer, wavelength dependency, and packet lifetime. Regarding the constraint of size of buffer being small, we set the buffer size B to be one-packet length (1500byte). The total amount of buffer in the optical packet switch is given by $B \times M$, thus the number of buffering port M is a key parameter to evaluate the benefits of optical RAM buffer in all-optical packet switch. The constraint of packet lifetime depends on strength of a bias light, so we change 150 ns of memory holding time assuming 250 μw for the bias power and increase it toward unlimited holding time. Note that unlimited holding time can be achieved when we use the optical bit memory based on semiconductor bistable lasers [11,12] where the power consumption is large. We compare the packet loss probabilities on optical packet switch having various number of buffering port M and compare the results without optical RAM buffer to see the effectiveness of buffering functionality.

3. 2 Simulation results

The traffic load ρ per wavelength is given by $\rho = \lambda/(\mu W)$ where λ is the total packet arrival rate at an input port and $1.0/\mu$ is the average packet length. In the simulation, the traffic load is set to 0.2 and packet length is set to 1500byte. The number of input/output ports N is set to 8, the number of wavelength per port is 8, and the transmission capacity of a wavelength is set to 40 Gbps. The packet lifetime L is set to 150 ns, 200 ns, and unlimited (∞). When a packet in the buffer cannot find available wavelength at output port, the packet is deleted from the buffer.

The packet loss probabilities dependent on the number of buffering port M is plotted in Fig. 4. For comparison purpose, the results of optical packet switch without using the optical RAM buffer (“WC-only”) is also plotted in the figure. We observe that when the number of buffering port is less than 10, there is no performance improvement by the optical RAM buffer. This is because most of packet losses occur due to the lack of buffering port. As the number of buffering port increases, the packet losses caused by the lack of buffering port decrease, which dominates the packet loss caused by the lack of wavelength resources on output port. More precisely, due to the lack of wavelength resources on output port, the packet in the optical RAM buffer exceeds the packet lifetime. Without the optical RAM buffer, the packet loss probability is greater than 10^{-4} regardless of the value of M. The packet loss probability with the optical RAM buffer improves more than two orders of magnitudes comparing the results without the optical RAM buffer. Looking at the impact of packet lifetime, we observe that InGaAsP-based photonic crystal (150ns packet lifetime) greatly improves the packet loss probability. If the packet lifetime is increased to 200ns, the packet loss probability is mostly the same to the results of the case when the optical RAM buffer has unlimited packet lifetime.

Fig. 5 shows the packet loss probabilities dependent on

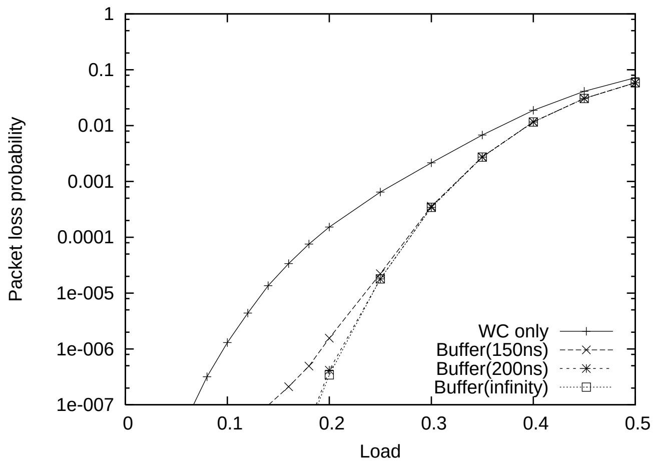

Figure 5 Packet loss probability dependent on the offered load ρ

the traffic load λ. As the figure indicates, the optical RAM buffer is not effective when the offered load is high. However, when the offered load is low (ρ <0.3), it is able to improve packet loss probability more than one order.

4. Concluding Remarks

Optical RAM buffer is vital devices for the optical packet switching. In this paper, we investigated the benefit of optical RAM buffer that employs an optical bistable device. We conducted computer simulations and evaluated the packet loss probability of optical packet switches. The results showed that the benefit of optical RAM buffer is significant when the offered load is low and when the number of buffering port is enough. A fact that ISP are not operating at high traffic load makes the optical RAM buffer to be a feasible solution for the future optical packet switched network.

We also investigated the impact of packet lifetime on the packet loss probability. The results indicated that InGaAsP-based photonic crystal cavities demonstrated in the recent paper certainly improve the packet loss probability. The results also indicated that extending the packet lifetime from 150 ns to 200ns will make the packet loss probability mostly the same to the results of unlimited packet lifetime.

Our future work is to minimize the power consumption of a bias light by considering the departure time of packets.

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References

[1] M. Murata and K. Kitayama, "Ultrafast photonic label switch for asynchronous packets of variable length," *in Proceedings of Infocom 2002*, vol. 1, pp. 371–380, 2002.

[2] T. Tanabe, M. Notomi, S. Mitsugi, A. Shinya, and E. Kuramochi, "Fast bistable all-optical switch and memory on a silicon photonic crystal on-chip," *Optics Letters*, vol. 30, Oct. 2005.

[3] R. Takahashi, "Recent progress in optical packet processing technologies for optical packet-switched networks," *NTT Technical Review*, vol. 2, July 2004.

[4] K. Kitayama, S. Arakawa, S. Matsuo, M. Murata, M. Notomi, R. Takahashi, and Y. Itaya, "All-optical RAM-based buffer for packet switch," in *in Proceedings of Photonics in Switching*, pp. 5–6, Aug. 2007.

[5] K. Kitayama, A. Shinya, S. Matsuo, R. Takahashi, M. Murata, and S. Arakawa, "Optical RAM buffer for all-optical packet switches," in *in Proceedings of Asia Communications and Photonics Conference and Exhibition (ACP)*, Nov. 2009.

[6] S. Yao, B. Mukherjee, S. J. B. Yoo, and S. Dixit, "A unified study of contention-resolution schemes in optical packet-switched networks," *Journal of Lightwave Technology*, vol. 21, no. 3, pp. 672–683, 2003.

[7] A. Shinya, S. Matsuo, Yosia, T. Tanabe, E. Kuramochi, T. Sato, T. Kakitsuka, and M. Notomi, "All-optical on-chip memory based on ultra high Q InGaAsP photonic crystal nanocavity," *in Proceedings of CLEO 2008*, p. CThJ4, 2008.

[8] M. Notomi, T. Tanabe, A. Shinya, E. Kuramochi, , and H. Taniyama, "On-chip all-optical switching and memory by silicon photonic crystal nanocavities," *Advances in Optical Technologies*, p. 10, 2008.

[9] K. Hamamoto, J. D. Merlier, M. Ohya, K. Shiba, K. Naniwae, S. Sudo, and T. Sasaki, "First demonstration of novel active multi-mode interferometer (MMI) LDs integrated with 1st order-mode permitted waveguides," *IEICE Electronics Express*, vol. 2, no. 13, pp. 399–403, 2005.

[10] R. Takahashi, T. Nakahara, K. Takahata, H. Takenouchi, T. Yasui, N. Kondo, and H. Suzuki, "Photonic random access memory using serial-to-parallel and parallel-to-serial conversion," in *Optical Fiber Communication Conference*, p. TuQ3, Optical Society of America, 2003.

[11] H. Kawaguchi, T. Mori, Y. Sato, and Y. Yamayoshi, "Optical buffer memory using polarization-bistable vertical-cavity surface-emitting lasers," *Japaese Journal of Applied Physics*, vol. 45, pp. L894–L897, Aug. 2006.

[12] M. Takenaka, M. Raburn, and Y. Nakano, "All-optical flip-flop multimode interference bistable laser diode," *IEEE Photonic Technology Letters*, vol. 17, pp. 968–970, May 2005.