Considerations on Packet Scheduling Algorithms for Photonic Packet Switch with WDM-FDL Buffers

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Abstract *We evaluate the performance of the photonic packet switch architecture to which advanced packet scheduling algorithms are applied and discuss the feasibility of the algorithms from the viewpoint of processing delay time.*

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Introduction

We evaluate the performance of photonic packet switch with WDM-based FDL (or WDM-FDL in short) supporting variable-length packets. We assume that all arriving packets are synchronized at the predefined time slot, and packet length is given by an integer multiple of the time slot. In this paper, we consider a shared buffer type switch, where all the packets, failing to acquire the output ports, are sent to the single FDL buffer attached to each output port. The advantage of the shared buffer type switch from the viewpoint of hardware cost has been discussed through the comparative evaluation between the shared buffer type switch and the output buffer type switch in [1]. As described above, the choice of the packet scheduling algorithm is crucial for enabling the photonic packet switch to achieve a high performance. We examine packet scheduling algorithms proposed in [2, 3] to the above packet switching architecture and evaluate the performance of the switch. Furthermore, we discuss the practical feasibility of the algorithms from the viewpoint of the processing delay time.

Photonic Packet Switch Architectures

The photonic packet switch that we consider in this paper accepts variable-length packets arriving asynchronously at the input port. Arriving packets are synchronized at a time with a predefined size. Figure 1 shows the architecture of the shared buffer type switch, which has one shared FDL buffer, and the packets are stored at the same buffer regardless of the destination output port. When the contention cannot be resolved by wavelength conversion, the packets are sent to the FDL buffer. When the contention of packets can be resolved by wavelength conversion, on the other hand, the packets are sent to the output ports directly. The shared buffer type switch has only one FDL buffer with W virtual input lines. The buffer size B_T is equal to B.

Packet Scheduling Algorithms

A packet scheduling algorithm is needed in order to determine the wavelength and FDL for the arriving packets. For each of the packets arriving within the time slot, the packet scheduler finds the appropriate wavelength and delay line as follows. If an unused wavelength on the output port is found, the packet is sent to the output port directly. When no wavelength is available at the output port, the appropriate FDL is found.

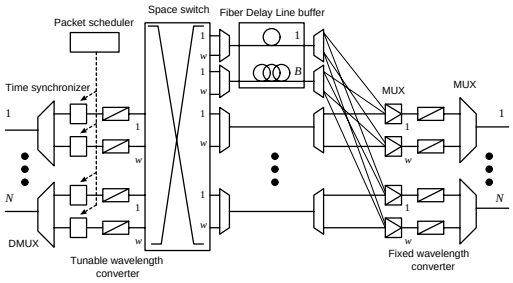

Figure 1: Shared buffer type photonic packet switch architecture

First, we introduce two simple original algorithms.

Algorithm A0: Assign the Wavelength in Round-Robin Fashion, which assigns the wavelength for packets arriving within the time slot in a round-robin fashion.

Algorithm A1: Assign to the Buffer with Minimum Queue, assigns the packet to the wavelength with the minimum queue length.

Since the shared buffer type switch has a single buffer, the queue length of the buffer becomes in long a high traffic load condition. Consequently the output interval between two packets destined for the same output port becomes large, and this is called the void space in this paper. The void space causes the low utilization of output ports. So, we propose new packet scheduling algorithm, called the ***void space reduction method***.

Void Space Reduction Method, which reduces the ill-effect of the void space by using wavelength conversion. The wavelength of the packet is converted such that the influence of the void space is minimized.

Performance of the Photonic Packet Switches

For the performance evaluation, the photonic packet switch and arriving traffic are modeled as follows. The numbers of input/output ports N and wavelengths on the fiber W are set to be 16 and 8, respectively. The wavelength capacity is 40 Gbps. A packet arrives according to the Poisson process. The average packet length is 400Bytes. The packet length

is exponentially distributed, but truncated at 1000Bytes. The time slot size is 20ns. the packet arrival rate is the same for all the input port, and the destination output port of the packet is chosen randomly. Figure 2 shows the simulation results of packet loss probability dependence on the buffer size B_T in the shared buffer type switch. In this figure, the performance of the switch degrades when the switch is equipped with a larger buffer. This is because the queue length becomes long and the possibility of a void space appearing becomes high. It can be observed that the performance is dramatically improved by introducing the void space reduction method.

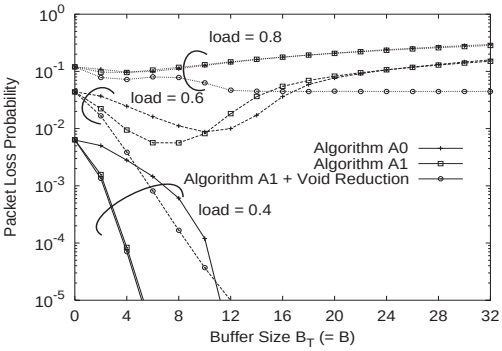

Figure 2: Packet loss probability (packet scheduling algorithms, load = 0.4, 0.6, and 0.8)

Feasibility of Packet Scheduling Algorithms

In order to consider the practical feasibility of packet scheduling algorithms, we design the hardware architecture for the algorithm using PLD design software. We measure the processing delay time of the algorithms through simulations. In Figure 3, we derive the processing delay time for packet scheduling algorithms.

One effective way of reducing the processing delay time is to decrease the number of wavelengths that the scheduler has to examine, because the processing delay time largely depends on the number of wavelength.

To realize this, we propose the ***wavelength grouping method***, which divides the wavelengths in a fiber into several groups and determines the group depending on the combination of its input port and output port for each packet. The wavelength in the selected group is assigned to a packet. Figure 4 shows the simulation results of packet loss probability in the switch to which the wavelength grouping method is applied. As shown in these figures, as the number of groups increases, the performance of a switch is degraded. For example, when the number of groups is more than 4, even the void space reduction method cannot achieve superior performance. Therefore, it is important to consider the trade-off between the performance of the switch and the processing delay time of packet scheduling algorithms. Therefore, using our proposed algorithm, we can achieve the best performance of the switch when the number of wavelengths is properly chosen according to the limitation of the hardware processing capability.

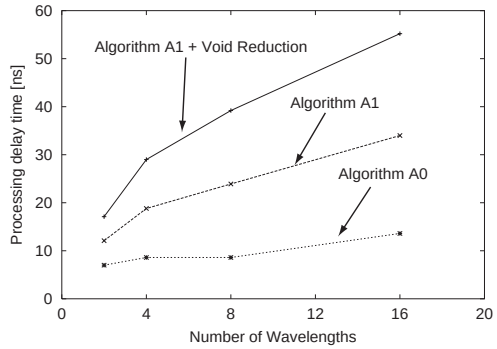

Figure 3: Processing delay times of packet scheduling algorithms

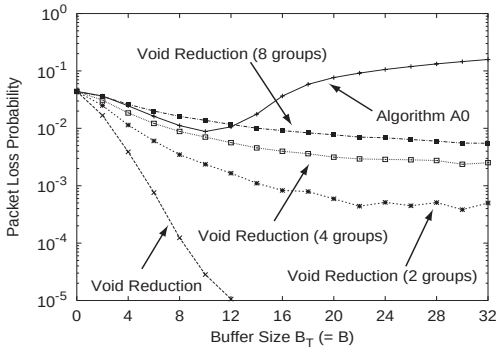

Figure 4: Packet loss probability (wavelength grouping method, load = 0.6)

Conclusions

We have evaluated the performance of the photonic packet switch architecture to which packet scheduling algorithms is applied with fiber delay line buffers which function as the shared buffer. We have proposed the void space reduction method, and the method could improve the performance of the shared buffer type switch. Furthermore, we have discussed the practical feasibility of packet scheduling algorithms from the viewpoint of processing delay time. Our wavelength grouping method decreased the processing delay time which depends on the number of wavelengths.

References

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